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Ultrafast-Programmable 2D Homojunctions Based on van der Waals Heterostructures on a Silicon Substrate

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The development of electrically ultrafast-programmable semiconductor homojunctions can lead to transformative multifunctional electronic devices. However, silicon-based homojunctions are not programmable so that alternative materials need to be explored. Here 2D, multi-functional, lateral homojunctions made of van der Waals heterostructures with a semi-floating-gate configuration on a p^{++} Si substrate feature atomically sharp interfaces and can be electrostatically programmed in nanoseconds, more than seven orders of magnitude faster than other 2D-based homojunctions. By applying voltage pulses with different polarities, lateral p—n, n^+—n and other types of homojunctions can be formed, varied, and reversed. The p—n homojunctions possess a high rectification ratio of up to ≈10^5 and can be dynamically switched between four distinct conduction states with the current spanning over nine orders of magnitude, enabling them to function as logic rectifiers, memories, and multi-valued logic inverters. Built on a p^{++} Si substrate, which acts as the control gate, the devices are compatible with Si technology.

1. Introduction

Semiconductor p-n junctions are the most fundamental device components in modern electronics and optoelectronics. Conventional p-n junctions are typically created by doping two adjacent regions of a semiconductor crystal with shallow donor and acceptor impurities by ion implantation, respectively. Such devices are not programmable and carrier transport is governed solely by the amplitude and polarity of the applied voltage bias across the junction. Moreover, for increased integration density, their performance degrades as their thickness enters the nanometer scale because the applicability and control of conventional doping and implantation techniques diminish. The advent of atomically thick 2D crystals enables the realization of p-n junctions at the ultimate thickness limit either by van der Waals stacking of 2D *p*- and *n*-type semiconductors[1] or by constructing homojunctions through electrostatic doping of the adjacent regions of 2D semiconductors with locally split-gate modulation,[2–4] ferroelectric polarization,[5,6] and semi-floating gate (SFG).[7,8] Such lateral or vertical van der Waals heterojunctions show diverse functions with superior performance in logic,[9–12] memories,[13–16] photodetectors,[17–19] and photovoltaic cells.[20,21] For example, benefitting from atomically sharp interfaces in van der Waals heterostructures, ultrafast, nanosecond-scale operation of nonvolatile, floating-gate memory devices has been realized.[14–16] However, there are still some inevitable issues in these van der Waals heterojunctions, such as the residual strain[22,23] and interlayer modulation.[24,25] In addition, band alignments of the heterostructures[26–28] could degrade charge transfer efficiency between 2D layers.[29] In contrast, homojunctions formed on a single 2D semiconductor possess continuous band bending, more uniform electrostatic-doping profile, easier electrically and optically programmable features, leading to larger rectification ratio,[7,30] better carrier mobility,[31] and more efficient photoresponse.[32,33] However, so far, 2D homojunctions controlled by ferroelectric polarization[5,6] or SFG[7,8] show long programming times on the order of milliseconds to seconds. Ultrafast-programmable 2D homojunctions remain elusive.

Here, we demonstrate that, with atomically sharp interfaces, semi-floating-gate-controlled 2D lateral homojunctions based on van der Waals heterostructures can be successfully programmed in ≈20 ns, which is more than 10^7 times faster than other homojunctions based on 2D materials.[7,8] The ultrafast-programmable 2D homojunctions exhibit a rectification ratio

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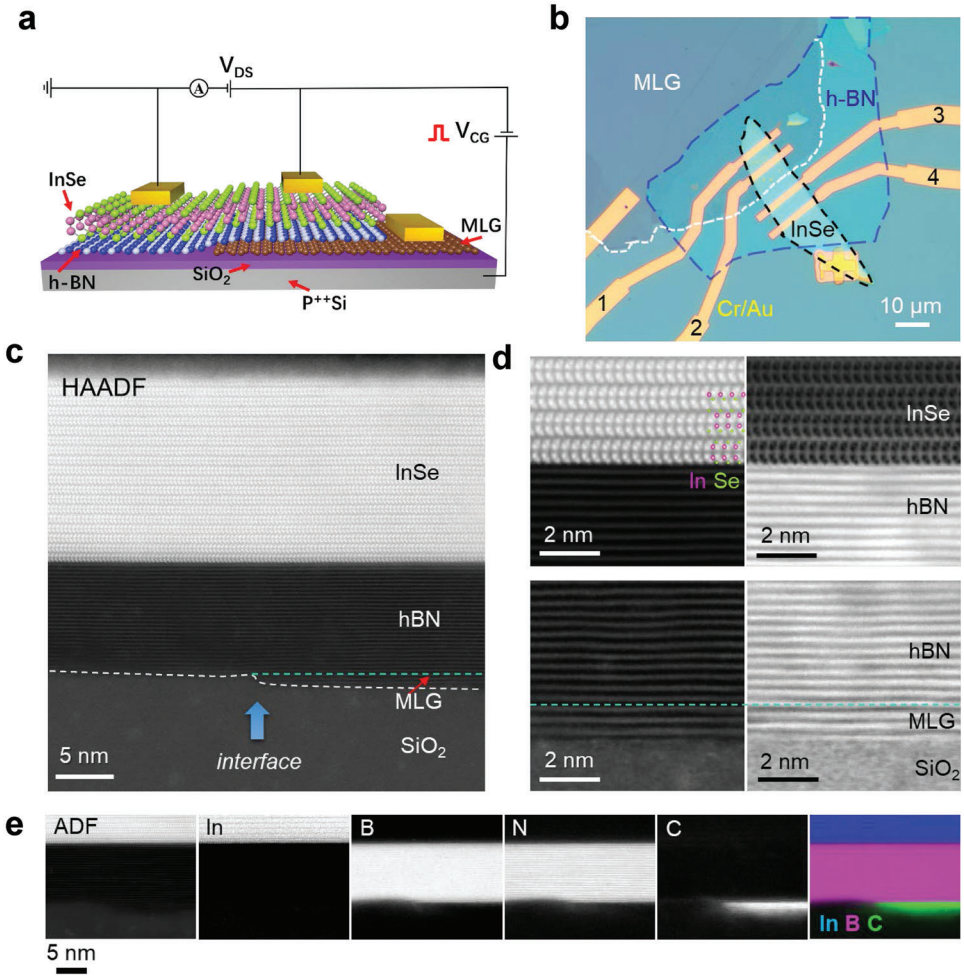


Figure 1. Ultrafast-programmable InSe homojunction with SFG configuration built upon van der Waals heterostructures. a) Schematic of an SFGconfiguration, in which only part of the InSe channel is aligned over the MLG to form an SFG architecture. b) Optical image of a typical SFG device based on InSe/hBN/MLG heterostructure placed on a SiO_2/Si substrate. The contact electrodes on the FG region and bare InSe region are labeled as (1, 2) and (3, 4), respectively. c) A large-scale HAADF-STEM image of the heterostructure on SiO_2. Atomically sharp interfaces between each functional layer can be clearly observed. d) Higher-resolution HAADF-STEM (left) and ABF (right) images acquired from the same heterostructure on different length scales, revealing clean interfaces without defects or contamination. Green and pink balls refer to selenium and indium atoms, respectively. e) EELS elemental mapping showing the uniform distribution of indium (In), boron (B), nitrogen (N), and carbon (C), respectively.

of ≈10^5 and four dynamically switchable non-volatile memory states. These lateral homojunctions are part of multilayer-graphene/hexagonal-boron-nitride (MLG/hBN) heterostructures with atomically sharp interfaces and chemical uniformity, as verified by atomic-resolution scanning transmission electron microscopy (STEM) imaging and electron-energy-loss spectroscopy (EELS). Such device configurations are further extended for designing reconfigurable logic applications and can be dynamically transformed between binary and ternary logics, showing great potential for electronic applications and multi-valued logics.

2. Results and Discussion

Figure 1a schematically shows the device configuration of a semi-floating gate field-effect transistor (SFGFET) based on a vertically stacked indium selenide (InSe)/hBN/MLG van der Waals heterostructure placed on a SiO_2/p^{++} Si substrate, in which InSe, hBN, MLG, SiO_2, and p^{++} Si are employed as the homojunction/channel material, tunneling layer, semi-floating gate, blocking layer and control gate, respectively. In a semi-floating-gate (SFG) configuration, only part of the InSe channel is stacked over the MLG floating gate. A metal electrode connected to the MLG floating gate outside of the channel part is used to enhance the gate coupling ratio to guarantee the ultrafast operation of the device.[14,15] The use of MLG as the floating gate can effectively reduce the floating-gate interference and suppress the ballistic transport of carriers across the floating gate along the *c*-axis.[34,35] Moreover, the high work function (≈4.6 eV) and high density of states of MLG independent of the layers ensure the stable storage of charges in the floating gate. An optical image of the SFGFET device is shown in Figure 1b. We first mechanically exfoliated MLG flakes (marked by the white dotted line) onto a SiO_2/p^{++} Si substrate. Afterward, mechanically exfoliated hBN (marked by the dark blue dotted line) and InSe flakes

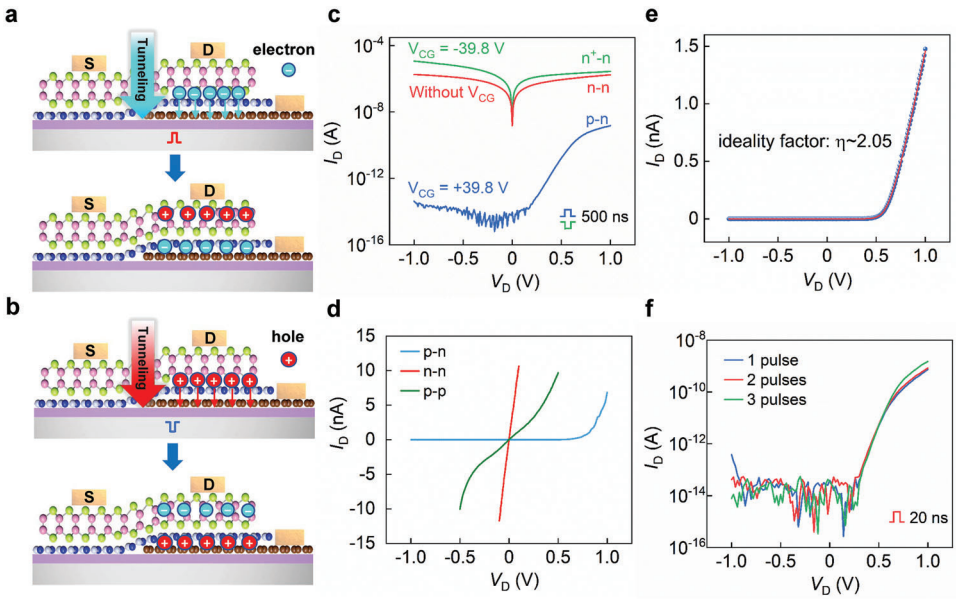


Figure 2. Ultrafast-programmable InSe homojunction with large rectification ratio. a,b) Schematic of charging the MLG semi-floating gate with electrons (a) or holes (b) by applying positive (a) or negative (b) voltage pulse on the Si control gate to program the InSe homojunction into different conduction states, respectively. c) Output (I_D–V_D) curves in logarithmic scale across the InSe homojunction without V_{CG} (red), after a 500 ns-wide voltage pulse of +39.8 V (blue) and −39.8 V (green) applied to Si control gate, respectively, showing the formation of n-n (red), p-n (blue), and n^+-n (green) junctions. d) I_D–V_D curves of the InSe homojunction formed between different contact electrodes (shown in Figure 1b) after a 160 ns-wide voltage pulse of +25.7 V applied to the Si control gate, showing the formation of p-p (green) (between electrodes 1 and 2), p-n (blue) (between electrodes 2 and 3), and n-n (red) (between electrodes 3 and 4) junctions, respectively. e) Linear plot of the I_D–V_D curve across the InSe p-n homojunction formed by applying a 500 ns-wide voltage pulse of +39.8 V to the Si control gate. The fitting curve (red line) based on a modified Shockley equation is consistent with the experimental result (blue balls), confirming the formation of the p-n junction. f) I_D–V_D curves across the InSe homojunction in logarithmic scale after 1 (blue), 2 (red), and 3 (green) voltage pulses with amplitude of +29.1 V and width of 20 ns applied to the Si control gate, respectively, showing the robustness of the formation of the p-n junction.

(marked by the black dotted lines) were sequentially stacked onto MLG by a dry transfer method, respectively.[14,36,37] Contact electrodes were defined by standard electron-beam lithography followed by electron-beam evaporation. The detailed device-fabrication processes are described in Experimental Section. Using the same device configuration by changing the channel material to molybdenum disulfide (MoS_2), van der Waals heterostructures of MoS_2/hBN/MLG with similar performance can also be fabricated, indicating that the device fabrication is reproducible.

We employed aberration-corrected STEM to characterize the interface quality of the SFG devices. Figure 1c shows a typical low-magnification cross-sectional, high-angle annular dark-field (HAADF) STEM image, featuring atomic-number contrast (Z-contrast) of the SFG device architecture. Figure 1d shows a set of atomic-resolution HAADF (left) and annular bright-field (ABF) (right) cross-sectional STEM images taken at the InSe/hBN and hBN/MLG/SiO_2 interfaces, revealing the atomically sharp and clean interfaces between each functional layer. An atomic model of InSe is overlaid on the upper left panel of Figure 1d, where pink and green balls represent indium and selenium atoms, respectively. The EELS mapping of the InSe/hBN/MLG heterostructure shown in Figure 1e clearly reveals the uniform distribution of indium, boron, nitrogen, and carbon elements and the chemically abrupt interfaces. These results unambiguously demonstrate the formation of extremely uniform, clean, and atomically sharp interfaces between different functional layers in our SFG devices without any observable residue gaps, defects, or contamination, which sets up a solid foundation for the realization of multifunctional electronic devices.

The InSe homojunction can be programmed by regulating the conductivity of the part of the InSe channel stacked over the MLG floating gate by applying a positive/negative voltage pulse to the p^{++} Si control gate, as schematically shown in **Figure 2**a,b, respectively. When applying a positive/negative voltage pulse to the control gate, electrons/holes tunnel through the hBN layer to the MLG floating gate via the Fowler–Nordheim (FN) tunneling mechanism. After the voltage pulse is removed, electrons/holes are trapped in the floating gate due to low back-tunneling probability,[14,15] resulting in the non-volatile hole/electron doping of the part of the InSe channel stacking over the floating-gate region and formation of p-n and n^+-n junctions, respectively. Figure 2c shows the typical output curves across the InSe homojunction at room temperature. When no voltage pulse is applied to the control gate (without V_{CG}, red curve), due to the unintentional electron doping of the InSe channel,[37] the InSe channel is free of electrostatic doping and behaves as an n-n homojunction with symmetric drain-source current (I_D) at negative and positive drain-source voltage (V_D) bias, respectively, indicating a good Ohmic contact is formed. In comparison, with a 500 ns-wide voltage pulse of +39.8 V applied (V_{CG} = +39.8 V, blue curve), an InSe p-n homojunction is formed and an apparent current rectification behavior with a high rectification ratio of ≈10^5 (V_D = ±1 V) is clearly presented. After applying a 500 ns-wide voltage pulse of −39.8 V (V_{CG} = −39.8 V, green curve), an

InSe n^+-n homojunction is formed and a weak reverse current rectification behavior with a rectification ratio of ≈4.2 occurs. The forward current of the InSe p-n homojunction increases monotonically when the amplitude of the control-gate voltage pulse is raised with the current-rectification behavior persisting (Figure S1, Supporting Information), indicating the robustness of such ultrafast programming nature of the InSe p-n homojunction.

The output behaviors of the InSe homojunction formed between different contact electrodes (Figure 2d) after applying a 160 ns-wide voltage pulse of +25.7 V reveal the formation of p-p (between electrodes 1 and 2), n-n (between electrodes 3 and 4), and p-n (between electrodes 2 and 3) junctions, respectively. The drain current in both the p-p and n-n junctions is much larger at small V_D than that in a p-n junction, indicating that the large rectification ratio (≈10^5) comes from the formation of a p-n junction rather than a Schottky junction.[2b] The linear plot of output characteristics across the InSe p-n homojunction (blue balls) after applying a 500 ns-wide voltage pulse of +39.8 V is shown in Figure 2e. It can be fitted by a modified Shockley equation including a series resistance R_s:[7,38]

$$I_D = \frac{\eta V_T}{R_S}\, W\left[\frac{I_0 R_S}{\eta V_T}\exp\left(\frac{V_D + I_0 R_S}{\eta V_T}\right)\right] - I_0 \quad (1)$$

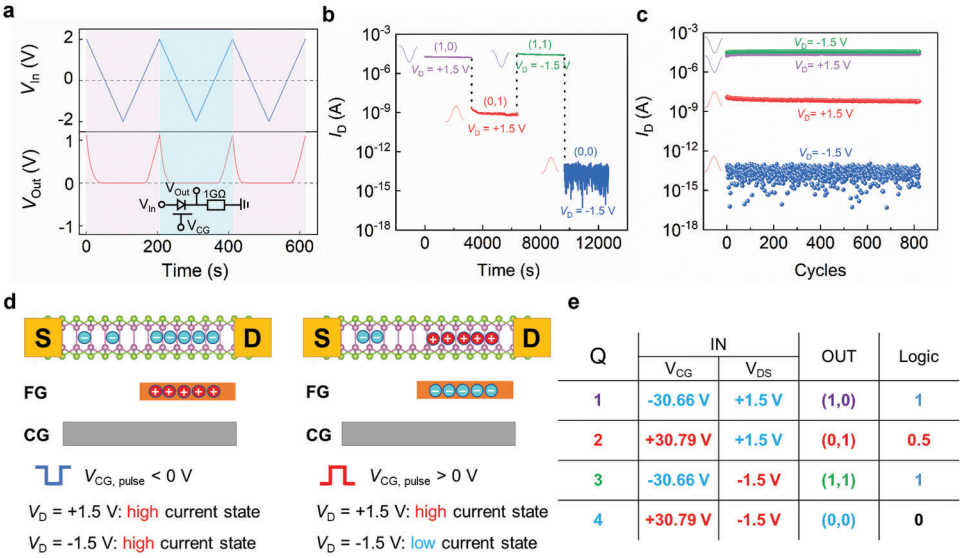
where η, V_T, I_0 refer to the ideality factor, $k_B T/e$, and the reverse-bias current, respectively. W is the Lambert W function, $k_B T/e$ is the thermal voltage at temperature T, k_B is the Boltzmann constant, and e is the electron charge. The series resistance R_s comes from the electrode/InSe contact.[7] We find that the fitting curve is fully consistent with the experimental data, further confirming the formation of the InSe p-n homojunction.

The transport mechanism across the p-n junction can be revealed by the value of the ideality factor (η). For ideal p-n junctions, when $\eta = 1$, the transport is governed by the diffusion process while when $\eta = 2$, the transport is dominated by recombination processes. The typical η for our InSe p-n homojunction is extracted as ≈2.05 (Figure 2e). All the ideality factors extracted from other devices are larger than 1 (Figure S2, Supporting Information), indicating that the transport is governed by recombination processes.[38] For InSe n^+-n homojunction programmed by negative $V_{CG,\,pulse}$, holes are accumulated in the floating-gate, which induces electron doping of the InSe channel above the floating-gate region and lateral n^+-n junction is formed. In this case, no holes are presented in the whole InSe channel, and no recombination current will be generated (Figure S3a, Supporting Information). The channel current mainly comes from electron drifting under a fixed voltage bias. For InSe p-n homojunction programmed by positive $V_{CG,\,pulse}$, electrons accumulated in floating-gate, which induces hole doping of the InSe channel above the floating-gate region and lateral p-n junction is formed. When the InSe p-n junction is biased, electrons and holes in different regions of the channel recombine together and the recombination current is generated in the depletion region (Figure S3b, Supporting Information). The ideality factor of ≈2.05 indicates that a large density of trap states is presented in the InSe channel and they act as recombination centers during electron transport,[7,39] which generates recombination current by elimination of electron-hole pairs. We have also employed an ultrafast voltage pulse of 20 ns with an amplitude of +29.1 V (the waveforms are shown in Figure S4, Supporting Information) to program the InSe homojunction. As shown in Figure 2f, after 1 pulse (blue), 2 pulses (red), and 3 pulses (green) are applied, the current rectification ratio remains as high as ≈10^5 in the InSe p-n homojunction, verifying the ultrafast-programmable capability of the InSe homojunction.

We have also performed computational simulations on the electron tunneling transport in the floating gate region dominated by the F-N tunneling process based on the quantum tunneling transport model (Note S1, Supporting Information). The calculated tunneling carrier density (n), electric field in the hBN layer ($|E_{BN}|$), tunneling current density (J), and the Fermi level shift (ΔE_F) as functions of the amplitudes and widths of the programming ($V_{CG} > 0$)/erasing ($V_{CG} < 0$) voltage pulses of our ultrafast-programmable InSe homojunctions are shown in Figure S5 (Supporting Information). For the pulse voltage of +29.1 V with 20 ns width for programming operation, n can reach a value larger than 10^{12} cm^{-2} (Figure S5a, Supporting Information), indicating the successful programming operation for the InSe homojunction.[40] E_{BN} is ≈15.5 MV cm^{-1} when a +30 or −30 V voltage pulse with 160 ns pulse width is applied, which is much larger than the threshold electric field of hBN of 7.94 MV cm^{-1},[41] confirming the domination of the F–N tunneling process when electrons/holes tunnel through the hBN layer.[14,15]

We have also calculated the Fermi level shift of the InSe channel (ΔE_F) over the floating-gate region when a positive V_{CG} is applied to the control gate (Note S2, Supporting Information). As shown in Figure S5d (Supporting Information), the midpoint of the InSe bandgap increases with the amplitude of V_{CG}. Notably, when ΔE_F exceeds 80 meV (marked by red dotted lines), an InSe p-n homojunction is formed. To reach this shift, for V_{CG} with a pulse width of 20 ns (black), 160 ns (red), and 500 ns (blue), the corresponding amplitudes are 24.0, 21.8, and 20.8 V, respectively, which are easily satisfied in our experiments. The good agreement between our experiments and theoretical calculations confirms the robustness of our ultrafast programming of InSe p-n homojunction. This robustness is further confirmed by the successful ultrafast programming of MoS_2 p-n homojunctions with a current rectification ratio of ≈10^5 when we replace the InSe channel material with MoS_2 (Figures S6,S7, Supporting Information). The theoretical calculations for MoS_2 devices also agree well with experiments due to the similar band structures between MoS_2 and InSe, as shown in Figure S8 (Supporting Information).

The ultrafast-programmable characteristics achievable in our van der Waals devices immediately establish a unique platform for novel device design and applications. For example, our ultrafast-programmable InSe p-n homojunction with a large rectification ratio of ≈10^5 allows us to rectify an input alternative triangular wave signal (V_{IN}). As shown in **Figure 3**a, the InSe homojunction programmed by a 500 ns-wide voltage pulse of +39.8 V behaves as a typical p-n diode (V_{OUT}), in which only the positive input voltage is allowed to pass through. When V_{IN} is negative, $V_{OUT} = 0$ V, indicating the successful rectification behavior for the input alternating signal. An equivalent circuit diagram with a loading resistor of 1 GΩ connected to the InSe p-n homojunction is shown in the inset. No observable changes in the current rectification behavior are present after changing the loading resistor to 5 GΩ, confirming the robustness of the current rectification



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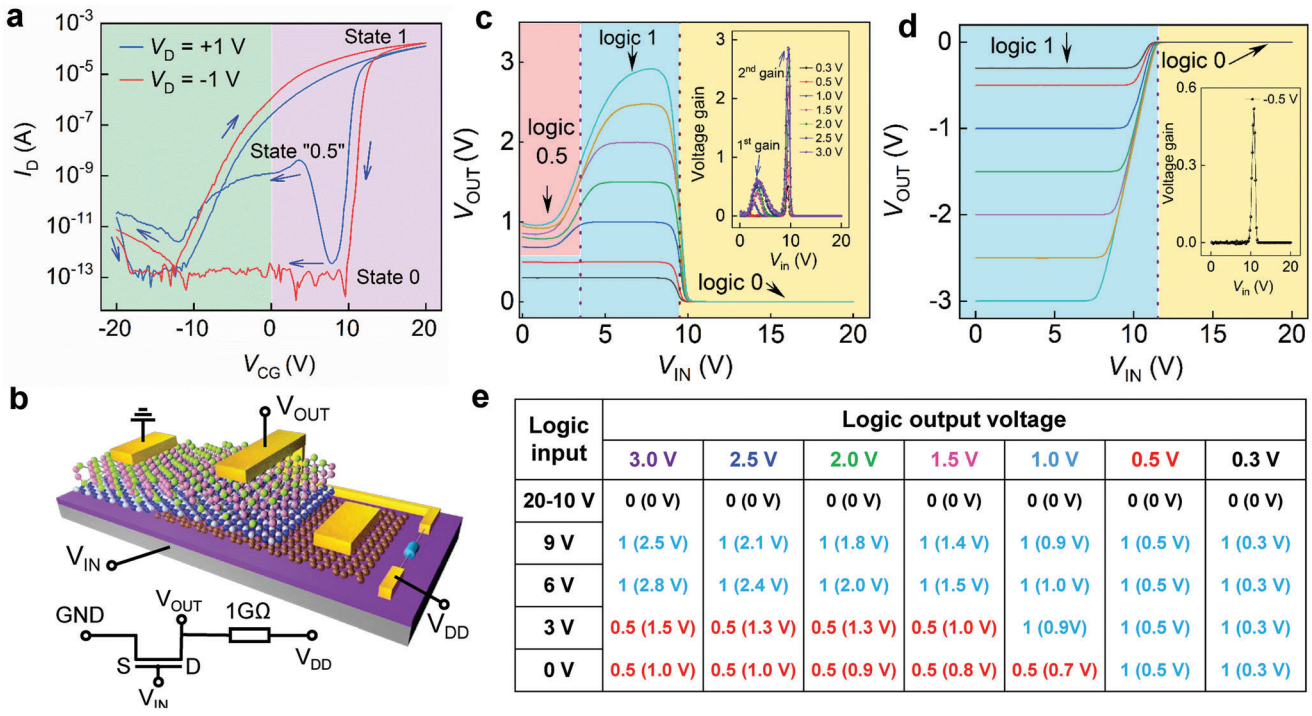
Q	IN		OUT	Logic
	V_{CG}	V_{DS}		
1	-30.66 V	+1.5 V	(1,0)	1
2	+30.79 V	+1.5 V	(0,1)	0.5
3	-30.66 V	-1.5 V	(1,1)	1
4	+30.79 V	-1.5 V	(0,0)	0

Figure 3. Ultrafast-programmable InSe homojunction for rectifiers and two-bit non-volatile memories. a) Output rectifying characteristics (V_{OUT}) of the InSe p-n homojunction programmed by a 500 ns-wide voltage pulse of +39.8 V with the input alternative triangular wave with an amplitude of 2 V (V_{IN}). The inset in the lower panel shows a schematic diagram of the rectifier circuit with a loading resistor of 1 GΩ connected to the InSe homojunction. b) Retention characteristics of the two-bit non-volatile memory by recording the time-evolution of four current states (I_D) across the InSe homojunction after applying one 160 ns-wide voltage pulse of V_{CG} = +30.79 or −30.66 V and reading I_D at V_D = ±1.5 V with V_{CG} = 0 V at room temperature (25 °C), respectively. c) Endurance performance of the two-bit non-volatile memory by cyclic switching the four current states across the InSe homojunction by applying a 160 ns-wide voltage pulse of V_{CG} = +30.79 or −30.66 V and reading I_D at V_D = ±1.5 V with V_{CG} = 0 V in one single cycle, respectively. d) Schematic of the working principle of the two-bit non-volatile memory, in which the device elements of the channel, drain (D) and source (S) contact electrodes (yellow boxes), floating gate (FG, orange bar), and control gate (CG, grey bar) are shown. Stored and induced positive (red) and negative (blue) charges in the channel and FG are indicated. e) Memory states (OUT) and logic states (Logic) in response to the input states (IN), showing the realization of ternary logic in the ultrafast-programmable InSe homojunction.

capability of our ultrafast-programmed InSe p-n homojunction (Figure S9, Supporting Information). Beyond the current rectifier, the successful ultrafast programming of InSe homojunction to four distinct conduction states enables them to work as two-bit non-volatile memories. The retention characteristics of the two-bit non-volatile memory are measured by recording the time-evolution behavior of the four conduction states after applying one 160 ns-wide voltage pulse of V_{CG} = +30.79 or −30.66 V and then reading I_D at V_D = ±1.5 V with V_{CG} = 0 V at room temperature in sequence, respectively. As shown in Figure 3b, the achieved four discernable conduction states (labeled as (1, 0), (0, 1), (1, 1), and (0, 0)) can still keep stable even after 3200 s. Such stability of the four conduction states presists even at temperatures as high as ≈85 °C, indicating the stable retention performance of our device when working as two-bit non-volatile memories. (Figure S10, Supporting Information). The endurance performance of the two-bit non-volatile memory is measured by cyclic switching of the four conduction states. In each cycle, the current is recorded after applying one 160 ns-wide voltage pulse of V_{CG} = +30.79 or −30.66 V and then reading I_D at V_D = ±1.5 V with V_{CG} = 0 V in sequence, respectively. As shown in Figure 3c, even after 820 cycles the four conduction states still persist, indicating the robust endurance performance of the two-bit non-volatile memory.

It should be noted that our two-bit non-volatile memory works based on the combination of ultrafast-programming/erasing the SFG with the alternative polarity of the reading-out voltages, which is completely different from that of traditional multi-bit floating-gate memories using various V_{CG}[42] or different numbers of voltage pulses[14] to change the number of charges stored in the floating gate. The apparent advantages of our two-bit non-volatile memory lie in that the multi-level current states are achieved through complete programing/erasing the stored charges in the floating gate by applying individual control-gate voltage pulse, ensuring the stability of the memory states. While in other ways, the stored charges in the floating gate are partially programmed/erased, leading to the possible instability in the multi-level current states. A schematic of the operating principles of the two-bit non-volatile memory is shown in Figure 3d. For $V_{CG, pulse}$ < 0 V, the InSe homojunction has been programmed to an n^+-n junction. High current states are achieved when reading I_D at both V_D = +1 V and V_D = −1 V (Figure 3b), respectively. While for $V_{CG, pulse}$ > 0 V, the InSe homojunction has been programmed to a p-n junction, high and low current states are achieved when reading I_D at V_D = +1 V and V_D = −1 V (Figure 3b), respectively. If we categorize the four current states by the polarity of the reading-out voltage, two independent binary current states with extinction ratios of ≈10^4 and ≈10^9 are obtained at a reading-out voltage of V_D = +1 and −1 V (Figure 3b), respectively, revealing the versatile operations of our two-bit non-volatile memory.

Figure 3e shows the memory states (OUT) and logic states (Logic) of the ultrafast-programmable InSe homojunction in response to the input states (IN), in which the memory states of (1, 0) and (1, 1) can be assigned as logic "1" state (high current state) and (0, 0) state (low current state) as logic "0" state, respectively,



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Logic input	Logic output voltage						
	3.0 V	2.5 V	2.0 V	1.5 V	1.0 V	0.5 V	0.3 V
20-10 V	0 (0 V)	0 (0 V)	0 (0 V)	0 (0 V)	0 (0 V)	0 (0 V)	0 (0 V)
9 V	1 (2.5 V)	1 (2.1 V)	1 (1.8 V)	1 (1.4 V)	1 (0.9 V)	1 (0.5 V)	1 (0.3 V)
6 V	1 (2.8 V)	1 (2.4 V)	1 (2.0 V)	1 (1.5 V)	1 (1.0 V)	1 (0.5 V)	1 (0.3 V)
3 V	0.5 (1.5 V)	0.5 (1.3 V)	0.5 (1.3 V)	0.5 (1.0 V)	1 (0.9V)	1 (0.5 V)	1 (0.3 V)
0 V	0.5 (1.0 V)	0.5 (1.0 V)	0.5 (0.9 V)	0.5 (0.8 V)	0.5 (0.7 V)	1 (0.5 V)	1 (0.3 V)

Figure 4. Multi-valued logic inverters based upon an InSe homojunction. a) Dual-sweeping transfer curves of the InSe homojunction at $V_D = \pm 1$ V, where three stable current states for $V_D = +1$ V (blue curve, state 1, state 0, and state "0.5") and two current states for $V_D = -1$ V (red curve, state 1 and state 0) can be clearly observed when sweeping V_{CG} from 20 to 0 V. b) Schematic diagram of the multi-valued logic inverter based on an InSe homojunction, in which the source electrode is grounded, drain and control gate electrodes are connected to the output and input terminals, respectively, V_{DD} is connected with a 1 GΩ resistor to drive the device. An equivalent circuit diagram is shown in the lower panel. c) Output curves of the logic inverter at various positive V_{DD} ($V_{DD} = 0.3$ V for black curve and then increases from 0.5 to 3 V in a step of 0.5 V), showing three different logic states, indicated by the yellow (logic 0), blue (logic 1), and red (logic 0.5) regions, respectively. The inset shows the first voltage gain (logic 0.5 / logic 1) and second voltage gain (logic 1 / logic 0) under different V_{DD}. d) Output curves of the logic inverter at various negative V_{DD} ($V_{DD} = -0.3$ V for black curve and then changes from −0.5 to −3 V in a step of −0.5 V), showing the binary logic states, represented by the yellow (logic 0) and blue (logic 1) regions, respectively. The inset shows a typical voltage gain at $V_{DD} = -0.5$ V. e) Summary of the output voltages and corresponding ternary logic states (logic 0, logic 0.5, and logic 1) in response to different positive V_{DD} and logic input of the InSe homojunction, the black, blue, and red colored text represent logic state 0, 1 and 0.5, respectively.

while the middle current state of (0, 1) can be assigned as a middle logic state of logic "0.5", indicating the realization of ternary logic, as will be discussed in the following part.

Digital inverters are one of the important elemental devices in integrated logic circuits. They comprise n-channel and p-channel FETs in series in complementary metal-oxide-semiconductor technology. Alternatively, in NMOS logic, replacing the PMOS FET either by a resistor or an n-channel FET working in depletion mode can also achieve the function of an inverter.[37] The realization of ternary logic in our ultrafast-programmable InSe homojunction (Figure 3e) enables the device to work as a multi-valued logic inverter. This inference is first justified by the transfer characteristic curves of the SFGFET device when dual sweeping V_{CG} from −20 to 20 V at both forward and reverse direction with $V_D = \pm 1$ V, respectively. As shown in **Figure 4**a, beyond the formation of large memory windows due to charge trapping in the MLG floating gate, three stable current states for $V_D = +1$ V (blue curve, state 1, state 0, and state "0.5"), and two current states for $V_D = -1$ V (red curve, state 1 and state 0) can be clearly observed when sweeping V_{CG} from 20 to 0 V, suggesting the operation of stable logic states in this region (pink). While sweeping V_{CG} from 0 to −20 V, no disguisible current levels are presented, indicating that this control-gate voltage range is not applicable for logic operations (green).

When sweeping V_{CG} from −20 to −10 V, holes are accumulated in the floating gate gradually and the whole InSe channel is mainly regulated by V_{CG}, inducing p-type doping in InSe with a low-current state and reaching the charge neutral point at $V_{CG} = -10$ V. When continuously sweeping V_{CG} from −10 to 0 V, the InSe channel over the floating-gate region (Channel region-I) is mainly regulated by the floating gate, while the other part of the InSe channel (Channel region-II) is regulated by V_{CG}. The number of electrons in Channel region-I is more than that of channel region-II, leading to the formation of the n^+-n junction. Two high current states at both $V_D = \pm 1$ V (μA current level) are observed when $V_{CG} = 0$ V. Further sweeping V_{CG} from 0 to 20 V, the decreased holes in the floating gate induce the slight decrease of electrons in Channel region-I, while the other part of the channel is electron-doped increasingly by V_{CG}, resulting in increases of the channel current until I_D is saturated at $V_{CG} = 20$ V (Figure S11a, Supporting Information). When sweeping V_{CG} back from 20 to 9 V, the increase in the number of electrons in the floating gate induces holes injection to Channel region-I, while the number of electrons in Channel region-II is decreased, leading

to the sharp decrease of the channel current (Figure S11b, Supporting Information). The Channel region-I reaches the charge neutral point again for 6 V < V_{CG} < 9 V and achieves the lowest current state. (Figure S11c, Supporting Information). Further sweeping V_{CG} from 6 to 0 V, Channel region-I is doped with holes and Channel region-II is still n-type doped, leading to the formation of the p-n homojunction. At V_{CG} = 0 V, for V_D = 1 V and V_D = −1 V, the p-n homojunction shows forward conducting and reverse cut-off behaviors, respectively, leading to two stable states, labeled as state 0.5 and state 0, respectively. When V_{CG} is swept from 0 to −11 V, the concentration of electrons in the floating gate gradually decreases, which induces the reduction of the depletion area of the p-n junction. The Channel region-II reaches the charge neutral point again at V_{CG} = −11 V (Figure S11e, Supporting Information). Further sweeping V_{CG} from −11 to −20 V increases hole doping in the whole InSe channel, leading to the increment of the current level (Figure S11f, Supporting Information). The dual-sweeping transfer curves under different sweeping directions and sweeping steps of control-gate voltage keep almost the same, suggesting the stability of the logic states, as shown in Figure S12 Supporting Information). Based on the three states for V_D = +1 V (State 1, State 0, and State "0.5") and two states for V_D = −1 V (State 1 and State 0) formed during back sweeping V_{CG} from 20 to 0 V, we can construct ternary and binary logic inverters only by tuning the polarity of the driving voltage.

The device configuration and electrical connections of the multi-valued digital inverter based upon the ultrafast-programmable InSe homojunction are schematically shown in Figure 4b, in which the bare InSe region (source electrode) is grounded, the InSe channel over the FG region (drain electrode) is connected to a 1 GΩ resistor and performs as the output terminal (V_{OUT}), while the control gate acts as input voltage terminal (V_{IN}). V_{DD} applied to the 1 GΩ resistor is used to drive the device. An equivalent circuit diagram is shown in the lower panel of Figure 4b. Ternary logic or binary logic in our InSe homojunction can be electrically programmed by simply switching the polarity of the driving voltage V_{DD}, as shown in the output curves of the logic inverter in Figure 4c,d, respectively. Notably, for V_{DD} = 0.3 and 0.5 V, the device works as a binary logic inverter (Figure 4c). Although when sweeping V_{IN} from 6 to 0 V, the InSe homojunction is programmed to a p-n junction, the low forward bias (V_{DD} = 0.3 and 0.5 V) induces a small current comparable to that of the depletion state when sweeping V_{IN} from 9 to 6 V (Figure S11c,d, Supporting Information), showing logic 1 state.

For comparison, the large forward bias ($V_{DD} \geq$ 1.5 V) drives the programmed InSe p-n homojunction to be turned on with a current level that is larger than the depletion state (6 V < V_{IN} < 9 V, logic 1), but smaller than that of the n^+-n InSe homojunction (11 V < V_{IN} < 20 V, logic 0) (Figure S11a,b, Supporting Information), showing intermediate logic 0.5 state. The inset shows the first and second voltage gain as a function of logic input (V_{IN}) under different driving voltages (V_{DD}). Apparently, the gain increases with V_{DD}, and the switching gains of the first and second logic states can reach up to 0.6 and 2.9 at V_{DD} = 3 V, respectively. Figure 4e summarizes the output voltage as functions of logic input and positive V_{DD}, indicating that the intermediate logic 0.5 state can be programmed by varying the amplitudes of driving voltage. For negative V_{DD}, when sweeping V_{IN} from 20 to 11 V and from 11 to 0 V, the InSe homojunction is programmed to n^+-n and reversely biased p-n junction (Figure 4a), respectively. The high and low current states in InSe n^+-n and p-n junctions are assigned as logic 0 and logic 1 states, respectively, as shown in Figure 4d. The inset shows a typical voltage gain as a function of logic input (V_{IN}) at V_{DD} = −0.5 V. The output voltage of this binary inverter under different negative V_{DD} and logic input (V_{IN}) is summarized in Table S1 (Supporting Information). Voltage gains of logic 0.5 to logic 1 (first gain) and logic 1 to logic 0 (second gain) as a function of V_{DD} are extracted and plotted in Figure S13 (Supporting Information). Both gains increase with increasing V_{DD}. Due to the NMOS nature of the multi-valued logic, the voltage gain is low compared to that of van der Waals heterostructures made by vertically stacking p- and n-type 2D semiconductors.[9,10] However, by simply tuning the polarity and amplitude of the driving voltage in our programmable InSe homojunction, ternary and binary logic can be realized. Further exploration of multi-valued logic could involve using thinner or high-k dielectric blocking layers to reduce the input voltage, thereby increasing the voltage gain and providing alternative design principles for subsequent logic circuits. The output characteristics of both ternary and binary logic inverters for input voltages with different program speed is shown in Figure S14 (Supporting Information). All the logic states keep stable under different input voltage steps, indicating that the intermediate results of the output voltage will not disrupt the other logic states. Due to the robust logic states in a single inverter with different program speeds of input voltage, when cascading two such inverter gates, it is expected that the logic states in each inverter gate will keep stable.

In our ultrafast-programable 2D InSe homojunction in semi-floating gate device architecture, multi-layered graphene is employed as a floating gate to address the interference issues between the floating gates of adjacent cells. However, as current device fabrication is based on the exfoliation method to form heterostructures, when scaling down, the device current could be possibly affected by the junction area, which can be a challenging issue. The successful scaling down of these ultrafast-programmable 2D homojunction devices is expected by combining the standard Si-based technology with the recently developed 3D Van der Waals integration methods or by introducing 3D device configuration as adopted in 3D-NAND flash technology.

3. Conclusion

In summary, we have fabricated ultrafast-programmable and multifunctional InSe homojunctions based on van der Waals heterostructures using a semi-floating-gate device architecture. The atomically sharp interfaces between the 2D functional layers in the van der Waals heterostructure play a key role in achieving ultrafast program operations. Lateral p-n, n^+-n, and other types of homojunctions can be formed and altered by simply tuning and reversing the polarities of the gate voltages. The formation of p-n homojunctions is confirmed by the theoretical calculations of the electron tunneling transport in the floating-gate region dominated by F–N tunneling processes based on the quantum transport model. Our ultrafast-programmable p-n homojunction with a rectification ratio of ≈10^5 and dynamically switchable four conduction states can function as logic rectifiers, memories, and multi-valued logic inverters. The robustness of the device

architecture is demonstrated when replacing the InSe channel material with MoS_2. Our ultrafast-programmable and multifunctional homojunctions based on van der Waals heterostructures provide new design protocols for the development of future electronic devices and could serve as indispensable building blocks of electronic memories, logic rectifiers, and integrated electronic devices in the next generation.

4. Experimental Section

Device Fabrication and Electrical Characterization: InSe, MoS_2, hBN, and graphite bulk crystals were purchased from 2D Semiconductors, SPI Supplies, HQ Graphene, and NGS Naturgraphit, respectively. InSe/hBN/MLG and MoS_2/hBN/MLG heterostructures were prepared on a silicon wafer with 300 nm SiO_2 using mechanical exfoliation and a dry-transfer approach. InSe was exfoliated and transferred in the glovebox with O_2 and H_2O concentrations below 0.1 ppm and MoS_2 was in the atmosphere. Then Cr/Au drain and source electrodes were defined by standard electron-beam lithography, electron-beam evaporation, and lift-off. The floating-gate memory devices were protected by a layer of spin-coated poly(methylmethacrylate) at once after lift-off. Electrical measurements were performed with a Keithley 4200 semiconductor characterization system (4200-SCS) and a homemade electric circuit in a vacuum probe station at room temperature. Electrical characterization of the voltage pulses with FWHM of 160 ns was performed in the 4200-SCS system equipped with 4225-PMU and 4225-RPM units. The ultrashort-voltage-pulse signals with full-width FWHM of ≈20 ns were generated from the home-built electrical circuits. The ultrahigh-speed characterization of semi-floating-gate memory devices was executed with the control-gate terminal connected to a home-made nanosecond voltage-pulse signal, while the drain terminals at the MLG side were connected to the 4200-SCS source measure units. The thicknesses of InSe, MoS_2, hBN, and MLG flakes were determined by a Bruker Dimension Edge atomic force microscope after all tests.

STEM Sample Preparation and Characterization: Before the focused ion beam and transmission electron microscope sample fabrication, the InSe/hBN/MLG SFGFET device placed on a SiO_2/Si substrate was protected by multilayered graphite flakes by the dry-transfer approach in the glove box. The process was to protect the InSe on the upper surface from being damaged by the ion beam with high energy during sample preparation. STEM samples for cross-sectional investigation were prepared using an FEI Helios NanoLab G3 CX focused-ion-beam system by the standard lift-out procedure. To minimize the sidewall damage and sufficiently thin the specimen for electron transparency, final milling was carried out at a voltage of 2 kV. Aberration-corrected STEM imaging was performed using a Nion HERMES-100 operated at 60 kV acceleration voltage and a probe forming a semi-angle of 32 mrad. HAADF and ABF imaging were acquired using annular detectors with a collection semi-angle of 75–210 and 30–15 mrad, respectively. EELS measurements were performed using a collection semi-angle of 75 mrad, an energy dispersion of 0.3 eV per channel, and a probe current of ≈20 pA. The B-K (188 eV), C-K (284 eV), N-K (401 eV), and In-M (443 eV) absorption edges were integrated for elemental mapping after background subtraction. The parent spectrum image was processed with the principal component analysis tool to reduce random noise.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

H.W., L.B., and R.G. contributed equally to this work. L.B. and H.-J.G. supervised the overall research. H.W., L.B., and H.-J.G. designed the experiments. H.W. and L.B. fabricated the devices and carried out the electrical measurements. R.A.G. and W.Z. performed the STEM analysis. A.W. and Q.H. constructed the homemade electric circuit with ultrashort voltage pulse signals with FWHM of 20 ns. H.W., L.B., W.K., W.Z., and S.T.P. analyzed the data. H.W., L.B., R.A.G., W.Z., S.T.P., and H.-J.G. wrote the paper. All the authors contributed to the preparation of the manuscript.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

2D homojunctions, logic rectifiers, multi-valued logic inverters, ultrafast programming, van der Waals heterostructures

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[1] A. K. Geim, I. V. Grigorieva, *Nature* **2013**, *499*, 419.
[2] B. W. H. Baugher, H. O. H. Churchill, Y. Yang, P. Jarillo-Herrero, *Nat. Nanotechnol.* **2014**, *9*, 262.
[3] Y.-Q. Bie, G. Grosso, M. Heuck, M. M. Furchi, Y. Cao, J. Zheng, D. Bunandar, E. Navarro-Moratalla, L. Zhou, D. K. Efetov, T. Taniguchi, K. Watanabe, J. Kong, D. Englund, P. Jarillo-Herrero, *Nat. Nanotechnol.* **2017**, *12*, 1124.
[4] C. Pan, C.-Y. Wang, S.-J. Liang, Y. Wang, T. Cao, P. Wang, C. Wang, S. Wang, B. Cheng, A. Gao, E. Liu, K. Watanabe, T. Taniguchi, F. Miao, *Nat. Electron.* **2020**, *3*, 383.
[5] G. J. Wu, X. D. Wang, Y. Chen, S. Q. Wu, B. M. Wu, Y. Y. Jiang, H. Shen, T. Lin, Q. Liu, X. R. Wang, P. Zhou, S. T. Zhang, W. D. Hu, X. J. Meng, J. H. Chu, J. L. Wang, *Adv. Mater.* **2020**, *32*, 1907937.
[6] G. Wu, B. Tian, L. Liu, W. Lv, S. Wu, X. Wang, Y. Chen, J. Li, Z. Wang, S. Wu, H. Shen, T. Lin, P. Zhou, Q. Liu, C. Duan, S. Zhang, X. Meng, S. Wu, W. Hu, X. Wang, J. Chu, J. Wang, *Nat. Electron.* **2020**, *3*, 43.
[7] D. Li, M. Y. Chen, Z. Z. Sun, P. Yu, Z. Liu, P. M. Ajayan, Z. X. Zhang, *Nat. Nanotechnol.* **2017**, *12*, 901.
[8] R. Cheng, L. Yin, F. Wang, Z. Wang, J. Wang, Y. Wen, W. Huang, M. G. Sendeku, L. Feng, Y. Liu, J. He, *Adv. Mater.* **2019**, *31*, 1901144.

[9] M. Q. Huang, S. M. Li, Z. F. Zhang, X. Xiong, X. F. Li, Y. Q. Wu, *Nat. Nanotechnol.* **2017**, *12*, 1148.
[10] A. Nourbakhsh, A. Zubair, M. S. Dresselhaus, T. Palacios, *Nano Lett.* **2016**, *16*, 1359.
[11] J. Shim, S. Oh, D.-H. Kang, S.-H. Jo, M. H. Ali, W.-Y. Choi, K. Heo, J. Jeon, S. Lee, M. Kim, Y. J. Song, J.-H. Park, *Nat. Commun.* **2016**, *7*, 13413.
[12] H. Chen, X. Xue, C. Liu, J. Fang, Z. Wang, J. Wang, D. W. Zhang, W. Hu, P. Zhou, *Nat. Electron.* **2021**, *4*, 399.
[13] C. S. Liu, X. Yan, X. F. Song, S. J. Ding, D. W. Zhang, P. Zhou, *Nat. Nanotechnol.* **2018**, *13*, 404.
[14] L. Wu, A. Wang, J. Shi, J. Yan, Z. Zhou, C. Bian, J. Ma, R. Ma, H. Liu, J. Chen, Y. Huang, W. Zhou, L. Bao, M. Ouyang, S. J. Pennycook, S. T. Pantelides, H.-J. Gao, *Nat. Nanotechnol.* **2021**, *16*, 882.
[15] L. Liu, C. Liu, L. Jiang, J. Li, Y. Ding, S. Wang, Y.-G. Jiang, Y.-B. Sun, J. Wang, S. Chen, D. W. Zhang, P. Zhou, *Nat. Nanotechnol.* **2021**, *16*, 874.
[16] Y. Li, Z. C. Zhang, J. Li, X.-D. Chen, Y. Kong, F.-D. Wang, G.-X. Zhang, T.-B. Lu, J. Zhang, *Nat. Commun.* **2022**, *13*, 4591.
[17] R. S. Yan, S. Fathipour, Y. M. Han, B. Song, S. D. Xiao, M. D. Li, N. Ma, V. Protasenko, D. A. Muller, D. Jena, H. G. Xing, *Nano Lett.* **2015**, *15*, 5791.
[18] F. Qin, F. Gao, M. Dai, Y. Hu, M. Yu, L. Wang, W. Feng, B. Li, P. Hu, *ACS Appl. Mater. Interfaces* **2020**, *12*, 37313.
[19] Y. Chen, Y. Wang, Z. Wang, Y. Gu, Y. Ye, X. Chai, J. Ye, Y. Chen, R. Xie, Y. Zhou, Z. Hu, Q. Li, L. Zhang, F. Wang, P. Wang, J. Miao, J. Wang, X. Chen, W. Lu, P. Zhou, W. Hu, *Nat. Electron.* **2021**, *4*, 357.
[20] L. Lv, F. Zhuge, F. Xie, X. Xiong, Q. Zhang, N. Zhang, Y. Huang, T. Zhai, *Nat. Commun.* **2019**, *10*, 3331.
[21] Y. X. Deng, Z. Luo, N. J. Conrad, H. Liu, Y. J. Gong, S. Najmaei, P. M. Ajayan, J. Lou, X. F. Xu, P. D. Ye, *ACS Nano* **2014**, *8*, 8292.
[22] C. D. Zhang, M. Y. Li, J. Tersoff, Y. M. Han, Y. S. Su, L. J. Li, D. A. Muller, C. K. Shih, *Nat. Nanotechnol.* **2018**, *13*, 152.
[23] M.-Y. Li, Y. Shi, C.-C. Cheng, L.-S. Lu, Y.-C. Lin, H.-L. Tang, M.-L. Tsai, C.-W. Chu, K.-H. Wei, J.-H. He, W.-H. Chang, K. Suenaga, L.-J. Li, *Science* **2015**, *349*, 524.
[24] Y. Zhang, L. Yin, J. Chu, T. A. Shifa, J. Xia, F. Wang, Y. Wen, X. Zhan, Z. Wang, J. He, *Adv. Mater.* **2018**, *30*, 1803665.
[25] X. Zhou, X. Hu, S. Zhou, H. Song, Q. Zhang, L. Pi, L. Li, H. Li, J. Lü, T. Zhai, *Adv. Mater.* **2018**, *30*, 1703286.
[26] M.-H. Chiu, C. Zhang, H.-W. Shiu, C.-P. Chuu, C.-H. Chen, C.-Y. S. Chang, C.-H. Chen, M.-Y. Chou, C.-K. Shih, L.-J. Li, *Nat. Commun.* **2015**, *6*, 7666.
[27] T. F. Yang, B. Y. Zheng, Z. Wang, T. Xu, C. Pan, J. Zou, X. H. Zhang, Z. Y. Qi, H. J. Liu, Y. X. Feng, W. D. Hu, F. Miao, L. T. Sun, X. F. Duan, A. L. Pan, *Nat. Commun.* **2017**, *8*, 1906.
[28] X. Liu, D. Qu, H.-M. Li, I. Moon, F. Ahmed, C. Kim, M. Lee, Y. Choi, J. H. Cho, J. C. Hone, W. J. Yoo, *ACS Nano* **2017**, *11*, 9143.
[29] A. A. Murthy, T. K. Stanev, J. D. Cain, S. Q. Hao, T. LaMountain, S. Kim, N. Speiser, K. Watanabe, T. Taniguchi, C. Wolverton, N. P. Stern, V. P. Dravid, *Nano Lett.* **2018**, *18*, 2990.
[30] Y. Jin, D. H. Keum, S. J. An, J. Kim, H. S. Lee, Y. Hee, *Adv. Mater.* **2015**, *27*, 5534.
[31] R. Kappera, D. Voiry, S. E. Yalcin, B. Branch, G. Gupta, A. D. Mohite, M. Chhowalla, *Nat. Mater.* **2014**, *13*, 1128.
[32] N. Huo, G. Konstantatos, *Nat. Commun.* **2017**, *8*, 572.
[33] J. C. Sun, Y. Y. Wang, S. Q. Guo, B. S. Wan, L. Q. Dong, Y. D. Gu, C. Song, C. F. Pan, Q. H. Zhang, L. Gu, F. Pan, J. Y. Zhang, *Adv. Mater.* **2020**, *32*, 1906499.
[34] L. Jae-Duk, H. Sung-Hoi, C. Jung-Dal, *IEEE Electron Device Lett.* **2002**, *23*, 264.
[35] A. Misra, H. Kalita, M. Waikar, A. Gour, M. Bhaisare, M. Khare, M. Aslam, A. Kottantharayil, presented at *2012 4th IEEE Int. Memory Workshop*, Milan, Italy, May **2012**.
[36] A. Castellanos-Gomez, M. Buscema, R. Molenaar, V. Singh, L. Janssen, H. S. J. van der Zant, G. A. Steele, *2D Mater.* **2014**, *1*, 011002.
[37] L. M. Wu, J. A. Shi, Z. Zhou, J. H. Yan, A. W. Wang, C. Bian, J. J. Ma, R. S. Ma, H. T. Liu, J. C. Chen, Y. Huang, W. Zhou, L. H. Bao, M. Ouyang, S. T. Pantelides, H. J. Gao, *Nano Res.* **2020**, *13*, 1127.
[38] T. C. Banwell, A. Jayakumar, *Electron. Lett.* **2000**, *36*, 291.
[39] A. Pospischil, M. M. Furchi, T. Mueller, *Nat. Nanotechnol.* **2014**, *9*, 257.
[40] D. Kahng, S. M. Sze, *Bell Syst. Tech. J.* **1967**, *46*, 1288.
[41] G.-H. Lee, Y.-J. Yu, C. Lee, C. Dean, K. L. Shepard, P. Kim, J. Hone, *Appl. Phys. Lett.* **2011**, *99*, 243114.
[42] C. Taehee, L. Yeong-Taek, K. Eun-Cheol, L. Jin-Wook, C. Sunmi, L. Seungjae, K. Dong-Hwan, H. Wook-Ghee, L. Young-Ho, L. Jae-Duk, C. Jung-Dal, S. Kang-Deog, *IEEE J. Solid-State Circuits* **2001**, *36*, 1700.